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Qualcomm, NC 5775 Morehouse Drive San Diego, CA 92121			NGO, NGUYEN HOANG	
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DATE MAILED: 09/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/973,249	Applicant(s) MOHSENI ET AL.	
	Examiner Nguyen Ngo	Art Unit 2663	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 09 October 2001.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-39 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-21, 23-34, 37 and 38 is/are rejected.
- 7) ☒ Claim(s) 22, 35, 36, and 39 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

1. Claims 1, 5, 7, 11, 15, 17, 26, 27, and 34 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As to claim 1, the term "a value" is vague and indefinite. Claims must be distinct and particularly point out subject matter. Examiner suggests explicitly naming the different values, e.g., first component value, second component value, delayed second component value, etc.

As for claim 5, 7, 11, 15, 17, 26, 27, and 34, the term "substantially" is vague and indefinite. Claims must be distinct and particularly point out subject matter.

Correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States

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only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-7, 11-17, 21, and 23-27 rejected under 35 U.S.C. 102(e) as being anticipated by Kawabe et al. (US 6377613), hereinafter referred to as Kawabe.

Regarding claim 1, Kawabe disclose a radio demodulation method employing QPSK so that a plurality of received signals are demodulated simultaneously (method of signal processing, col2 lines4-8). Kawabe further discloses;

that the employed radio frequency modulation method be QPSK where base band spread spectrum signals are divided into an I signal and a Q signal (col10 lines 50-55). From figure 1, Kawabe further discloses of receiving digital base band spread spectrum signals, which the first and second spread spectrum signals received at the antennas are entered into a multiplexer (receiving a composite signal having a first component and a second component (I and Q signal), col3 lines 65- col4 lines 7). From figure 2b, Kawabe discloses the I/O timing chart of the multiplexer, which shows a antenna 1 signal (first component or I signal) and a antenna 2 signal (second component or Q signal), the antenna 1 signal having data values for each chip period (D11, D12, D13, D14...) and the antenna 2 signal also having data values for each chip period (D21, D22, D23, D24...). It is further seen from figure 2b, that the value of the antenna 1 signal and the value of the antenna 2 signal start at the beginning of the chip period (the first component including a value during each of the series of time periods (D11, D12, etc.), and the second component including a value (D21, D22, etc.) having a first time relation to a corresponding value of the first component during each of the

series of time periods (starting at the beginning of the chip periods), 212, and 213 of figure 2b).

of a multiplexer output, including the delayed antenna 2 signal (producing a delayed second component). From figure 2b, Kawabe shows the multiplexer output having a D11 and a D21 component in the first chip period. It is apparent that the D21 component of the multiplexer output (214 of figure 2b) is the delayed version of the antenna 2 signal during the 1st period (producing a delayed second component (D21 in multiplexer 214 output) including a value having a second time relation (D21 being half a period delayed as seen in figure 2b) value of the first component during each of the series of time periods).

of a multiplexer output, carrying the antenna 1 and 2 signals (multiplexing the values of the delayed second component and the values of a component based on the first component onto a common signal path, 214 multiplexer output of figure 2b).

Regarding claim 2, Kawabe discloses all the limitations as seen in figure 2b and the rejection of claim 1.

Regarding claim 3, Kawabe discloses from figure 2b of chip periods being equal durations. D11 of antenna 1 signal taking up the first chip period, D12 taking up the second chip period, and etc. (series of consecutive time periods of equal duration).

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Regarding claim 4 and 5, Kawabe discloses from figure 2b that the first time relation is that D11 and D21 starts at the beginning of the period, and that the second time relation is that the delayed D21 starts half a period later than the beginning of the period or D11. The difference is thus one-half a period. (a difference between the second time relation and the first time relation is measured in durations of a time period and includes an integer portion and a nonzero fractional portion, and wherein the fractional portion is at least one-quarter of a time period and no greater than three-quarters of a time period (one-half a period), figure 2b).

Regarding claim 6, Kawabe discloses from figure 2b of a divided clock, which defines the boundaries of a chip period (a boundary between each of the series of time periods is defined by a transition of a clock signal, 211 Divided Clock).

Regarding claim 7, Kawabe discloses from figure 2b of a duty cycle of the clock signal being substantially to fifty percent.

Regarding claim 11, Kawabe disclose a radio demodulation method employing QPSK so that a plurality of received signals are demodulated simultaneously (method of signal processing, col2 lines4-8). Kawabe further discloses;

that the employed radio frequency modulation method be QPSK where base band spread spectrum signals are divided into an I signal and a Q signal (col10 lines 50-55). From figure 1, Kawabe further discloses of receiving digital base band spread

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spectrum signals, which the first and second spread spectrum signals received at the antennas are entered into a multiplexer (receiving a composite signal having a first component and a second component (I and Q signal), col3 lines 65- col4 lines 7). From figure 2b, Kawabe discloses the I/O timing chart of the multiplexer, which shows a antenna 1 signal (first component or I signal) and a antenna 2 signal (second component or Q signal), the antenna 1 signal having data values for each chip period (D11, D12, D13, D14... corresponding to the first component including a series of values, each value of the first component being constant over substantially an entire corresponding one of a series of time periods) and the antenna 2 signal also having data values for each chip period (D21, D22, D23, D24... corresponding to the second component including a series of values, each value of the second component being constant over substantially an entire corresponding one of a series of time periods). It is further seen from figure 2b, that the value of the antenna 1 signal and the value of the antenna 2 signal start at the beginning of the chip period (the first component including a value during each of the series of time periods (D11, D12, etc.), and the second component including a value (D21, D22, etc.) having a first time relation to a corresponding value of the first component during each of the series of time periods (starting at the beginning of the chip periods), 212, and 213 of figure 2b).

of a multiplexer output, including the delayed antenna 2 signal (producing a delayed second component based on the second component). From figure 2b, Kawabe shows the multiplexer output having a D11 and a D21 component in the first chip period. It is apparent that the D21 component of the multiplexer output (214 of figure

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2b) is the delayed version of the antenna 2 signal during the 1st period (producing a delayed second component (D21 in multiplexer 214 output) based on the second component and having a fractional delay with respect to the second component (D21 being half a period delayed as seen in figure 2b) the delayed second component including a series of values, each value of the delayed second component being constant over substantially an entire corresponding one of the series of time periods (D21, D22, D23 and etc of the multiplexer output of figure 2b)).

of a multiplexer output, carrying the antenna 1 and 2 signals (multiplexing the values of the delayed second component and the values of a component based on the first component onto a common signal path, 214 multiplexer output of figure 2b).

Regarding claim 12, Kawabe discloses all the limitations as seen in figure 2b and the rejection of claim 11.

Regarding claim 13, Kawabe discloses from figure 2b of chip periods being equal durations. D11 of antenna 1 signal taking up the first chip period, D12 taking up the second chip period, and etc. (series of consecutive time periods of equal duration).

Regarding claim 14 and 15, Kawabe discloses from figure 2b that the first time relation is that D11 and D21 starts at the beginning of the period, and that the second time relation is that the delayed D21 starts half a period later then the beginning of the period or D11. The difference is thus one-half a period. (a difference between the second time

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relation and the first time relation is measured in durations of a time period and includes an integer portion and a nonzero fractional portion, and wherein the fractional portion is at least one-quarter of a time period and no greater than three-quarters of a time period (one-half a period), figure 2b).

Regarding claim 16, Kawabe discloses from figure 2b of a divided clock, which defines the boundaries of a chip period (a boundary between each of the series of time periods is defined by a transition of a clock signal, 211 Divided Clock).

Regarding claim 17, Kawabe discloses from figure 2b of a duty cycle of the clock signal being substantially to fifty percent.

Regarding claim 21, Kawabe discloses from figure 16 of a de-multiplexer 2545, which de-multiplexes the output coming from the multiplexer 2509 into Acc. Registers (2546-2549 of figure 16) corresponding to demultiplexing the values of the delayed second component and the first component. The multiplexer output being the delayed second component and the value of the component based on the first component from the common signal path (as seen in 1703 multiplexer 2509 output of figure 17). Access Timing For Accumulation Registers (1709-1712) further shows the produced transferred first component based on the first component and a transferred second component based on the second component as seen in figure 17.

Kawabe further discloses of a multiplier (2543 multiplier of figure 16) that multiplies a I code and Q code (2540 and 2541 code generators) with the output of multiplexer 2509 (modulating an in-phase component of a carrier with a component based on the transferred first component and a quadrature component of the carrier with a component based on the transferred second component).

Regarding claim 23, Kawabe disclose a radio demodulation method employing QPSK so that a plurality of received signals are demodulated simultaneously (method comprising, col2 lines4-8). Kawabe further discloses;

that the employed radio frequency modulation method be QPSK where base band spread spectrum signals are divided into an I signal and a Q signal (col10 lines 50-55). From figure 1, Kawabe further discloses of receiving digital base band spread spectrum signals, which the first and second spread spectrum signals received at the antennas are entered into a multiplexer (receiving a composite signal having a first component and a second component (I and Q signal), col3 lines 65- col4 lines 7).

of a multiplexer output, carrying the antenna 1 and 2 signals (transmitting a second composite signal (multiplex output) having a first component and a second component (antenna 1 and 2 signals), 214 multiplexer output of figure 2b).

that from figure 2b, Kawabe discloses the I/O timing chart of the multiplexer, which shows a antenna 1 signal (first component or I signal) and a antenna 2 signal (second component or Q signal), the antenna 1 signal having data values for each chip period (D11, D12, D13, D14...) and the antenna 2 signal also having data values for

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each chip period (D21, D22, D23, D24...). It is further seen from figure 2b, that the value of the antenna 1 signal and the value of the antenna 2 signal start at the beginning of the chip period or divided clock cycle (stream of digital data information carried over the first component of the first composite signal (D11, D12, D13, D14...) is synchronous with a clock signal and has a first time relation (both starting at the beginning of a period or clock cycle) to a stream of digital information carried over the second component of the first composite signal (D21, D22, D23, D24...)).

of a multiplexer output, including the delayed antenna 2 signal (producing a delayed second component). From figure 2b, Kawabe shows the multiplexer output having a D11 and a D21 component in the first chip period. It is apparent that the D21 component of the multiplexer output (214 of figure 2b) is the delayed version (half a period) of the antenna 2 signal during the 1st period (stream of digital information carried over the first component of the first composite signal is synchronous with the clock signal (D11, D12, D13, D14... which starts at the beginning of a period or clock cycle) and has a second time relation to a stream of digital information carried over the second component of the second composite signal (D21, D22, D23, D24... delayed versions of signal 2 being half a period delayed from D11, D12, D13, D14 of antenna 1 signal)).

that the multiplexer output, including antenna 1 signal and delayed antenna 2 signal are based on the original antenna 1 signal and antenna 2 signal as it is seen from figure 2b (wherein the stream of digital information carried over the first component of the second composite signal (multiplexer output) is based on the stream of digital information carried over the first component (antenna 1 signal) of the first composite

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signal and wherein the stream of digital information carried over the second component of the second composite signal (multiplex output) is based on the stream of digital information carried over the second component of the first composite signal (antenna 2 signal)).

that the first relation being that signal 1 and signal 2 values start at the beginning of the period or clock cycle and the second relation being that signal 1 and delayed signal 2 start half a period from each other as seen from figure 2b (wherein the first time relation is different from the second time relation).

Regarding claim 24, Kawabe discloses all the limitations as seen in figure 2b and the rejection of claim 23.

Regarding claim 25 and 26, Kawabe discloses from figure 2b that the first time relation is that D11 and D21 starts at the beginning of the period, and that the second time relation is that the delayed D21 starts half a period later then the beginning of the period or D11. The difference is thus one-half a period. (a difference between the second time relation and the first time relation is measured in durations of a time period and includes an integer portion and a nonzero fractional portion, and wherein the fractional portion is at least one-quarter of a time period and no greater than three-quarters of a time period (one-half a period), figure 2b).

Regarding claim 27, Kawabe discloses from figure 2b of a duty cycle of the clock signal being substantially to fifty percent.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. Claims 8, 9, 10, 18, 19, 20, 28, 29, 30-34, and 37-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kawabe et al. (US 6377613), hereafter referred to as Kawabe.

Regarding claim 8, Kawabe discloses from figure 2b of an antenna 1 signal and antenna 2 signal having values of D11, D12, and etc. and D21, D22, and etc, respectively (values multiplexed onto the common signal path). It should be obvious to a person skilled in the art that these values are n bits wide, and is further seen from the

multiplexed output that the output is less than $2n$ bits wide. (common signal path that multiplexes the values of the two signals).

Regarding claim 9, Kawabe discloses from figure 2b of an antenna 1 signal and antenna 2 signal having values of D11, D12, and etc. and D21, D22, and etc, respectively (values multiplexed onto the common signal path). It should be obvious to a person skilled in the art that these values are n bits wide, and is further seen from the multiplexed output that the output is less than $2n$ bits wide. (common signal path that multiplexes the values of the two signals). It would further be obvious to change the common signal path to n bits wide, as this is simply a parameter that may be changed by the system.

Regarding claim 10, Kawabe fails to disclose the delaying of a first component. But it would be obvious to a person skilled in the art to be able to delay the first component with the same method and apparatus for delaying the second component to efficiently multiplex the two components.

Regarding claim 18, Kawabe discloses from figure 2b of an antenna 1 signal and antenna 2 signal having values of D11, D12, and etc. and D21, D22, and etc, respectively (values multiplexed onto the common signal path). It should be obvious to a person skilled in the art that these values are n bits wide, and is further seen from the

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multiplexed output that the output is less than $2n$ bits wide. (common signal path that multiplexes the values of the two signals).

Regarding claim 19, Kawabe discloses from figure 2b of an antenna 1 signal and antenna 2 signal having values of D11, D12, and etc. and D21, D22, and etc, respectively (values multiplexed onto the common signal path). It should be obvious to a person skilled in the art that these values are n bits wide, and is further seen from the multiplexed output that the output is less than $2n$ bits wide. (common signal path that multiplexes the values of the two signals). It would further be obvious to change the common signal path to n bits wide, as this is simply a parameter that may be changed by the system.

Regarding claim 20, Kawabe fails to disclose the delaying of a first component. But it would be obvious to a person skilled in the art to be able to delay the first component with the same method and apparatus for delaying the second component to efficiently multiplex the two components.

Regarding claim 28, Kawabe discloses from figure 2b of an antenna 1 signal and antenna 2 signal having values of D11, D12, and etc. and D21, D22, and etc, respectively (values multiplexed onto the common signal path). It should be obvious to a person skilled in the art that these values are n bits wide, and is further seen from the

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multiplexed output that the output is less than $2n$ bits wide. (common signal path that multiplexes the values of the two signals).

Regarding claim 29, Kawabe discloses from figure 2b of an antenna 1 signal and antenna 2 signal having values of D11, D12, and etc. and D21, D22, and etc, respectively (values multiplexed onto the common signal path). It should be obvious to a person skilled in the art that these values are n bits wide, and is further seen from the multiplexed output that the output is less than $2n$ bits wide. (common signal path that multiplexes the values of the two signals). It would further be obvious to change the common signal path to n bits wide, as this is simply a parameter that may be changed by the system.

Regarding claim 30, Kawabe discloses a communication apparatus that multiplex base band signals in a time division manner (device configured to output multiplexed signals based on an original composite signal having a first component and a second component, abstract). Kawabe further discloses;

a multiplexer output (a common signal path configured and arranged to carry the multiplexed signal, 214 multiplexer output of figure 2b)

a multiplexer (104 multiplexer of figure 1) that receives digital base band spread spectrum signals, which the first and second spread spectrum signals received at the antennas are entered into a multiplexer (a multiplexer configured and arranged to receive a component based on the first component (antenna 1 signal) and a delayed

second component based on the second component (output of 204 AND gate of figure 2a) and to produce the multiplexed signal, col3 lines 65- col4 lines 7).

Kawabe however fails to disclose the specific limitation of having a filter configured and arranged to receive the second component and to produce the delayed second component. Kawabe however discloses of an AND gate (204 of figure 2a) that produces the delayed antenna 2 signal (delayed second component). It would thus be obvious to a person skilled in the art to exchange a filter for a AND gate to produce the same results of delaying the second component.

Regarding claim 31, Kawabe discloses the limitations of claim 31 as seen from figure 1. Figure 1 discloses the output of multiplexer 104 to be connected to different terminal of the chip package and further discloses of a chip period (the common signal path includes a plurality of terminals of a chip package that includes the device).

Regarding claim 32, Kawabe fails to disclose the delaying of a first component. But it would be obvious to a person skilled in the art to be able to delay the first component with the same method and apparatus for delaying the second component to efficiently multiplex the two components.

Regarding claim 33 and 34, Kawabe discloses from figure 2b that the first time relation is that D11 and D21 starts at the beginning of the period, and that the second time relation is that the delayed D21 starts half a period later then the beginning of the period

or D11. The difference is thus one-half a period. (a difference between the second time relation and the first time relation is measured in durations of a time period and includes an integer portion and a nonzero fractional portion, and wherein the fractional portion is at least one-quarter of a time period and no greater than three-quarters of a time period (one-half a period), figure 2b).

Regarding claim 37, Kawabe discloses a communication apparatus that multiplex base band signals in a time division manner (a device configured and arranged to output a multiplexed signal based on an original composite signal having a first component and a second component, abstract). Kawabe further discloses;

a multiplexer output (a common signal path configured and arranged to carry the multiplexed signal, 214 multiplexer output of figure 2b)

a multiplexer (104 multiplexer of figure 1) that receives digital base band spread spectrum signals, which the first and second spread spectrum signals received at the antennas are entered into a multiplexer (a multiplexer configured and arranged to receive a component based on the first component (antenna 1 signal) and a delayed second component based on the second component (output of 204 AND gate of figure 2a) and to produce the multiplexed signal, col3 lines 65- col4 lines 7).

of a de-multiplexer as seen in figure 16 (2545 de-multiplexer), which de-multiplexes the output coming from the multiplexer 2509 into Acc. Registers (2546-2549 of figure 16) corresponding to de-multiplexing the values of the delayed second component and the first component. The multiplexer output being the delayed second

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component and the value of the component based on the first component from the common signal path (as seen in 1703 multiplexer 2509 output of figure 17). Access Timing For Accumulation Registers (1709-1712) further shows the produced transferred first component based on the first component and a transferred second component based on the second component as seen in figure 17 (a demultiplexer configured and arranged to receive the multiplexed signal and to produce a transferred component based on the first component and a transferred component based on the delayed second component).

that from figure 2b that the first time relation is that D11 and D21 starts at the beginning of the period, and that the second time relation is that the delayed D21 starts half a period later then the beginning of the period or D11. The difference is thus one-half a period. (wherein the delayed second component is synchronous to the first component and has a fractional delay with respect to the second component, figure 2b).

Kawabe however fails to disclose the specific limitation of having a filter configured and arranged to receive the second component and to produce the delayed second component. Kawabe however discloses of an AND gate (204 of figure 2a) that produces the delayed antenna 2 signal (delayed second component). It would thus be obvious to a person skilled in the art to exchange a filter for a AND gate to produce the same results of delaying the second component.

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Regarding claim 38, Kawabe discloses of a multiplier (2543 multiplier of figure 16) that multiplies a I code and Q code (2540 and 2541 code generators) with the output of multiplexer 2509 (modulator configured and arrange to modulate an in-phase component of a carrier with a component based on the transferred first component and a quadrature component of the carrier with a component based on the transferred second component).

Allowable Subject Matter

7. Claims 22, 35, 36, and 39 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. Claims 22 and 39 are allowable due to the further limitations of producing a first analog component based on the transferred first component and a second analog component based on the transferred second component.

9. Claims 35 are allowable due to the further limitations the shifted value being equal to 2^I times the input value where I is an integer and wherein a value of the delayed second component is based on the shifted value.

10. Claims 36 are allowable due to the further limitations of the transfer function of the filter.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) Wakamori et al. (US 5408474), Apparatus For Multiplexing Digital Video and A Digital Sub-Signal And Method Thereof.

b) Ten Kate et al. (U.S 5481643), Transmitter, Receiver, And Record Carrier For Transmitting/Receiving At Least A First And A Second Signal Component.

c) Andrew et al. (US 4723237), Signal Transmission Arrangement, A Transmitter And A Receiver For Such An Arrangement And A Communication System Including Such an Arrangement.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nguyen Ngo whose telephone number is (571) 272-8398. The examiner can normally be reached on Monday-Friday 7am - 3:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ricky Ngo can be reached on (571) 272-3139. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.


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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

N.N

Nguyen Ngo

United States Patent & Trademark Office
Patent Examiner AU 2663
(571) 272-8398


RICKY NGO
PRIMARY EXAMINER

9/27/05